AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

In the claims

Claim 1 (previously presented) A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

switch means disposed on said substrate for selectively interconnecting said inputs to said outputs, said switch means having M multiplexers and a plurality (N) switchable amplifiers, each of said switchable amplifier operatively coupled to a corresponding one of said N inputs; and

means disposed on said substrate for controlling said switch means,

wherein each multiplexer is an N to 1 multiplexer and each multiplexer is adapted to receive each of said N electrical inputs,

wherein each of said N inputs to each of said multiplexer is received through a respective one of said N switchable amplifiers, and

wherein one of the N inputs can be selected for outputting to one of the M outputs by switching on the corresponding switchable amplifiers and disabling the rest of the switchable amplifiers.

Claim 2-3 (canceled)

Claim 4 (previously presented) The invention of Claim 1, wherein the switch means further comprise a plurality (N) of isolation buffers, each of said isolation buffers operatively coupled to the output of a corresponding one of switchable amplifiers.

Claim 5 (previously presented) A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

switch means disposed on said substrate for selectively interconnecting said inputs to said outputs, said switch means having M multiplexers; and

means disposed on said substrate for controlling said switch means,

wherein each multiplexer includes N selection multiplexers.

Claim 6 (original) The invention of Claim 5 further including means for summing the outputs of said N selection multiplexers to provide a single output.

Claim 7 (original)The invention of Claim 6 further including means for buffering said single output.

Claim 8 (canceled)

Claim 9 (currently amended) A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

switch means disposed on said substrate for selectively interconnecting said plurality of electrical inputs to said plurality of electrical outputs, said switch means having M multiplexers; and

means disposed on said substrate for controlling said switch means~~; and~~

~~means for summing the outputs of said N buffers to provide a single output,~~

wherein each multiplexer includes N selection multiplexers, and

wherein each of said N inputs to each of said N selection multiplexers is received through a respective one of N switchable isolation buffers.

Claim 10 (original) The invention of Claim 9 further including means for buffering said single output.

Claim 11 (original) The invention of Claim 1 wherein said control means includes a serial in, parallel out shift register.

Claim 12 (canceled)

Claim 15 (currently amended) A crosspoint switch architecture having:

a monolithic substrate;

a plurality (N) of electrical inputs provided on said substrate;

a plurality (M) of electrical outputs provided on said substrate;

M multiplexers disposed on said substrate for selectively interconnecting said plurality of electrical inputs to said plurality of electrical outputs, each of said multiplexers being an N to 1 multiplexer, whereby each multiplexer is adapted to receive each of said plurality of electrical inputs; and

a serial in, parallel out shift register disposed on said substrate for controlling said multiplexers,; ~~and~~

~~means for summing the outputs of said N buffers to provide a single output.~~

wherein each multiplexer includes N selection multiplexers

Claim 16 (original) The invention of Claim 15 further including means for buffering said single output.

Claim 17-18 (canceled)